

JAPANESE PATENT OFFICE
PATENT JOURNAL
KOKAI PATENT APPLICATION NO. HEI 8[1996]-125112

Technical Disclosure Section

Int. Cl. ⁶ :	H 01 L	25/065 25/07 25/18 H 01 L	25/08
Application No.:	Hei 6[1994]-262130		
Application Date:	October 26, 1994		
Publication Date:	May 17, 1996		
No. of Claims:	6(Total of 8 pages; OL)		
Examination Request:	Not requested		

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Inventor:	Takahisa Nishima Hitachi Super SI Engineering K.K. 5-20-1 Kamimizu Motomachi Ohira-shi, Tokyo
Applicants:	000005108 Hitachi Corp. 4-6 Kandasurugadai Chiyoda-ku, Tokyo

000233468
Hitachi Super LSI
Engineering K.K.
5-20-1 Kamimizu Motomachi
Ohira-shi, Tokyo

Agent:

Okazu Sasai,
patent attorney

[There are no amendments to this patent.]

Abstract

Purpose

To enable the mounting in layers of semiconductor elements with various configurations, without constraints on the configurations or positional relationships of the individual semiconductor elements.

Constitution

A semiconductor device in which balls 3a, 3b are formed by nailhead bonding on pads 2a, 2b of a first semiconductor element 1a and a second semiconductor element 1b, the two [elements] having the same dimensions, and bumps 4a, 4b are obtained by pressing down on the formed balls 3a, 3b, and after the flattened bump 4a of the first semiconductor element 1a is connected to lead 5a which is supported by carrier tape 5b, the remaining bump 4a and bump 4b formed on the second semiconductor element 1b are bonded directly by heat pressurization.

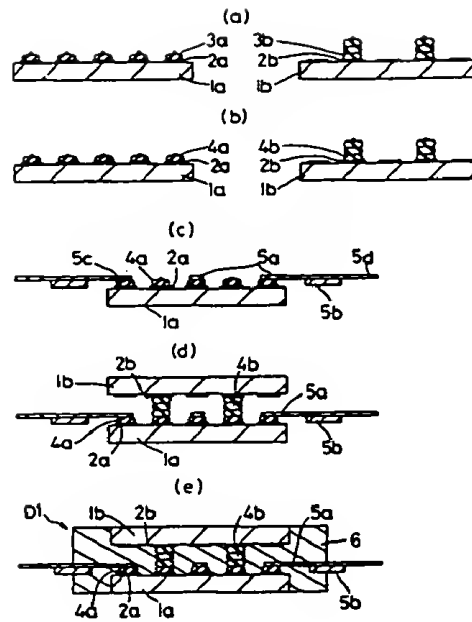


Figure 1

Key: 1a First semiconductor element
 1b Second semiconductor element
 2a Pad
 2b Pad
 3a Ball
 3b Ball
 4a Bump
 4b Bump
 5a Lead
 5b Carrier tape
 5c Inner terminal section
 5d Outer terminal section
 6 Resin

Claims

1. A semiconductor device characterized in that it comprises a first semiconductor element that is connected to the inner terminal section of a lead by means of a first bump, and a second semiconductor element that opposes said first semiconductor element through said lead, and is connected to said first semiconductor element by means of said lead or by means of a second bump that is greater than the width of the support structure of said lead.

2. The semiconductor device of Claim 1, characterized in that the support structure of said lead is a carrier tape of the TAB process, and the height of said second bump is made greater than the thickness of said carrier tape.

3. The semiconductor device of Claim 1 or 2, characterized in that, with the opposite sides of said first and second semiconductor elements exposed, the bonding position with respect to said lead is sealed with resin.

4. Manufacturing method for a semiconductor device characterized in that it comprises a first process in which a first and a second bump are formed on the bonding pad for the first and the second semiconductor element, a second process in which said first semiconductor element is connected to the inner terminal section of the lead by means of the first bump, and a third process in which, by means of a second bump whose height is greater than the thickness of said lead or the support structure of said lead, said first semiconductor element is connected to said second semiconductor element in an orientation in which they are in opposition through the lead.

5. Manufacturing method for a semiconductor device of Claim 4, characterized in that subsequent to the third process, a fourth process occurs in which, with the opposite sides of said first and second semiconductor elements exposed, the bonding position, which includes said first and second bumps, is sealed with resin.

6. Manufacturing method for a semiconductor device of Claim 4 or Claim 5, characterized in that said first and second bumps are formed in one step or multiple steps with nail bonding that utilizes at least one of heat energy or ultrasound energy.

★ ★ ★